REMARKS

Claims 1-48 are pending and stand rejected. The Examiner's reconsideration of the rejections in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-10, 11-19, and 20-29, and 30-39 were rejected under 35 U.S.C. §103(a) over Funk in view of Dias et al. (U.S. Patent 5,010,331). The Examiner stated essentially that Dias teaches a processor connected through N data lines ("control data" lines) to a "logic unit" and "that there are many more M **data** lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig. 1.2) than N **data** lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig. 1.2)." Applicant maintains that the indicated signal lines of Dias are not N "**data** lines" as that term is conventionally defined and understood by persons skilled in the art to differ from the "control lines" in the claims as amended.

Claims 31, 35-36, 40, and 44-45 were rejected under 35 U.S.C. §102(b) as anticipated by Funk et al., U.S. Patent 6,026,119. The Examiner stated essentially that Funk teaches all the limitations recited in claims 31, 35-36, including: a "processor bus" having "address lines", a "packet bus" for controlling an RF modem, and a master controller connected to both (between) those two busses, the master controller being provided for issuing "command packets" (i.e., "packetized commands") for controlling the modem (or a plurality of peripherals) through the N data lines of the packet bus. The applicant respectfully submits that Funk does not disclose a "packet bus" being operatively connected to the "master controller", nor a "packet bus" for controlling an RF modem (nor a memory thereof).

As the Examiner has acknowledged "Funk et al. fails to clearly teach where M data lines is greater than N data lines", (Office Action, Page 4). Funk (U.S. Patent 6,026,119) does not teach nor suggest a bus data-width change (M down to N) between the processor and the modem, where the modem bus has N data lines while the processor bus has M data lines, where M is greater than N, as claimed in independent claims 1, 11, 21, 31, and 40 and in the claims depending therefrom (in all the claims). Funk teaches only that N is equal to M among the data lines between the modem and the processor, and further, Funk contains no suggestion nor any motivation to eliminate some (M minus N) data lines from the M = N data communication path "430, 432" between the modem and the processor shown in FIG. 4 of Funk. Instead, Funk equates the M data lines in bus (430) as being the same as the N data lines in bus (432) since Funk characterizes the entire bus "430, 432" between the processor and the "logic unit" (107, Fig. 4) of the RF modem (101) as one single "data and control" bus "430, 432" (see Col. 5, lines 4-7). Thus, Funk entirely fails to teach N "data lines for conveying ... a data packet including the M bits of data" from the M data lines of the processor bus, wherein "M is greater than N", as substantially claimed in claims 1-50 (all the claims) herein.

Funk does not teach an N-bit wide "packet bus" (distinct from the "processor bus" having address lines) anywhere between the M-bit wide processor bus (421) and the modem (101), as claimed in claims 1, 11, 21, 31, and 40 and claims depending therefrom (all the claims). Therefore Funk fails to teach or suggest all the limitations of claims 1-50.

Further, applicant respectfully submits that Dias does not teach nor suggest a processor bus having "M data lines ... wherein ... the M data lines convey M bits of data in parallel" and "a packet bus having: ... N bidirectional data lines for conveying ... a data packet including the M bits of data." Even if, assuming *arguendo,* that Dias teaches "wherein M is greater than N", Dias does not teach that the N supposed "data lines" convey "the M bits of data" from the "M data lines" of the supposed processor bus.

The "N data lines 1.22, 1.26, 1.28 (Fig. 1.2) going to the control logic unit 1.30 (Fig 1.2)" in Dias as referred to by the Examiner simply do not transmit the M bits of data that are transmitted over the "M data lines 1.17 (Fig. 1.2) going to the processor 1.14 (Fig 1.2)" in Dias referred to by the Examiner. Dias does NOT teach nor suggest a processor bus having address lines and M data lines carrying M bits of data being reduced or "packed" down into a "packet bus" (nor any other sort of bus) having fewer-than-M (N) "data lines." Thus, neither Funk nor Dias teaches "M data lines" for carrying M bits of data being greater than "N data lines" for carrying the same M bits of data.

Moreover, neither Dias nor Funk et al. (U.S. Patent 6,026,119) teaches or suggests a memory or a modem or a "master controller" on or operatively connected to a "packet bus" having N data lines (N being less than the data width M of the processor's Data/Address line bus). Accordingly, claims 1-10, 11-19, and 20-29, and 30-39, 40-47, 48-49 are not rendered obvious over Funk in view of Dias.

Additionally, since Funk teaches that each of the Processor-RAM bus (436) and the Processor-Modem bus ("430, 432") contains both dedicated "data" lines and dedicated "control" lines including address lines (i.e., each is a conventional "data and

control" processor bus including address lines), Funk does not teach or suggest sending a "command packet" (i.e., "packetized command") having some control functions over the N "data" lines of the Processor-Modem bus ("430, 432").

And as indicated in Figs. 5 and 7 and the corresponding text in Funk, the "controller interface"(111) does not add a "command packet" (i.e., "packetized commands") to the data it receives from the processor, nor does the "controller interface" (111) format or modify any data at all. Thus, the "controller interface" (111) does not "issue" "command packets" (i.e., "packetized commands") nor does it in any way control any peripheral by issuing any "command packets" (i.e., "packetized commands") a claimed in claims 1-48 including independent claims 1, 11, 21, 31, and 40.

Therefore, Funk does not teach or suggest a master controller or any other element between the processor (421) and the modem (101), inserting (e.g., "issuing", Claim 40), nor any bus conveying a "command packet" as claimed in claims 1, 11, 21, 31, and 40.

Claims 2-10, and 49 & 50 depend from claim 1. Claims 12-19 depend from claim 11. Claims 22-30 depend from claim 21. Claims 32-39 depend from claim 31. The dependent claims are believed to be allowable for at least the reasons given for claims 1, 11, 21, 31 and 40.

For the forgoing reasons, the application, including claims 1-50, is believed to be in condition for allowance. Early and favorable action is respectfully urged.

Respectfully submitted,

By: _____

Frank Chau
Reg. No. 34,136
Attorney for Applicant(s)

Mailing Address:
F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, New York 11797
TEL: (516) 692-8888
FAX: (516) 692-8889